



The figure consists of nine timing diagrams, labeled 1 through 9, arranged horizontally. Each diagram shows a clock signal (represented by a square wave) and a data signal (represented by a step function). The diagrams illustrate different timing relationships between the clock and data signals, such as setup and hold times, and data validity relative to the clock edges. Diagram 1 shows a data signal that is valid before and after the clock edge. Diagram 2 shows a data signal that is valid during the clock edge. Diagram 3 shows a data signal that is valid after the clock edge. Diagram 4 shows a data signal that is valid during the clock edge. Diagram 5 shows a data signal that is valid during the clock edge. Diagram 6 shows a data signal that is valid during the clock edge. Diagram 7 shows a data signal that is valid during the clock edge. Diagram 8 shows a data signal that is valid during the clock edge. Diagram 9 shows a high-frequency clock signal with a data signal that is valid during the clock edge.





